Storage ECC

IPM-ECC

BCH Encoder/Decoder IP Core

Key Features

- ECC for NandFlash Storage
  - Up to 76 error-bits/block
  - Configurable block size
- Fully Configurable
  - Latency
  - Datapath
  - Error number
  - Packet size

Benefits

- Full hardware implementation for maximum performance, encoding, error detection and correction
- Balanced performance/gatecount
- All Galois fields covered
- Validated IP reduces Time-To-Market

Evaluation

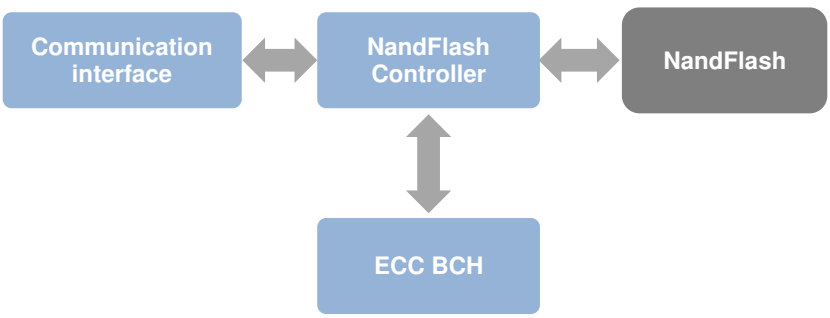
- Full features
- Simulation testbench
- Evaluation package for FPGA

Deliverables

- Verilog RTL source code
- Synthesis scripts
- Technical documentation
- Technical support

Overview

Nand Flash write cycles are limited. An ECC detects and corrects failed operations, increasing the lifetime of the Nand Flash memory. For Nand Flash-based data storage, using an ECC is mandatory to ensuring data validity. IP-Maker's powerful ECC is based on the BCH algorithm. The IP-Maker BCH Encoder/Decoder is full-featured with ease-of-use in FPGA and SoC designs.



ECC BCH in a storage system

The IP-Maker BCH Encoder/Decoder is fully configurable, allowing to it reach the best latency or the smallest footprint. Customizable parameters include: Chien Search algorithm, Galois Field, and data path. The IP-Maker BCH Encoder/Decoder IP Core is delivered in Verilog RTL that can be implemented in an ASIC or FPGA. It is fully tested with test bench models and hardware tested with FPGAs. The package includes Verilog RTL code, technical documentation, and a complete test environment.

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